WHAT IS CLAIMED IS:

1. A varactor, comprising:

a second type substrate;

two gate structures, disposed over the second type substrate, each of the gate structures comprising an inter-gate dielectric layer and a gate conductive layer on the inter-gate dielectric layer;

a first type doped region, disposed in the second type substrate between the two gate structures; and

a second type doped region, disposed in the second type substrate at a side of the two gate structures apart from the first type doped region;

wherein the first type doped region is electrically connected to a first electrode, and the second type doped region is electrically connected to a second electrode, and the two gate structures are electrically connected with the first electrode or the second electrode.

2. The varactor of claim 1, wherein the first type doped region is a p-type doped region, and the second type doped region is an n-type doped region.

3. The varactor of claim 1, wherein the first type doped region is an n-type doped region, and the second type doped region is a p-type doped region.

4. The varactor of claim 1, further comprising:

a polycide layer, disposed over the gate conductive layer, the first type doped region and the second type doped region.

5. The varactor of claim 1, further comprising:

a first type lightly doped region, disposed in the second type substrate adjacent to the first type doped region; and

a second type lightly doped region, disposed in the second type substrate adjacent to the second type doped region.

6. The varactor of claim 5, further comprising:

a spacer, disposed over a sidewall of each of the gate structures covering the first type lightly doped region and the second type lightly doped region.

7. A differential varactor, comprising:

at least one pair of varactors, disposed over a second type substrate, wherein each of the varactors comprising:

a first varactor, the first varactor comprising:

two first gate structures, disposed over the second type substrate and each of the first gate structures comprising a first inter-gate dielectric layer and a first gate conductive layer on the first inter-gate dielectric layer;

a first type first doped region, disposed in the second type substrate between the two first gate structures; and

a second type first doped region, disposed in the second type substrate at a side of the two first gate structures apart from the first type first doped region; and

a second varactor, adjacent to the first varactor, the second varactor comprising:

two second gate structures, disposed over the second type substrate, and each of the second gate structures comprises a second inter-gate dielectric layer and a second gate conductive layer on the second inter-gate dielectric layer;

a first type second doped region, disposed in the second type substrate between the two second gate structures; and

a second type second doped region, disposed in the second type substrate at a side of the two second gate structures apart from the first type second doped region, wherein the second type second doped region is adjacent to the second type first doped region,

wherein, the first gate structure and the first type first doped region are electrically connected to a tuning voltage, and the second gate structure and the first type second doped region are electrically connected to a relative tuning voltage, and the second type first doped region and the second type second doped region are grounded.

8. The differential varactor of claim 7, wherein the first type first doped region and the first type second doped region are p-type doped regions, and the second type first doped region and the second type second doped region are n-type doped regions.

9. The differential varactor of claim 7, wherein the first type first doped region and the first type second doped region are n-type doped regions, and the second type first doped region and the second type second doped region are p-type doped regions.

10. The differential varactor of claim 7, further comprising:

a polycide layer, disposed over the first gate conductive layer, the second gate conductive layer, the first type first doped region, the first type second doped region, the second type first doped region and the second type second doped region.

11. The differential varactor of claim 7, further comprising:

a first type lightly doped region, disposed in the second type substrate adjacent to the first type first doped region; and

a second type lightly doped region, disposed in the second type substrate adjacent to the second type first doped region .

12. The differential varactor of claim 11, further comprising:

a spacer, disposed over a sidewall of each of the first gate structures covering the first type lightly doped region and the second type lightly doped region.

13. The differential varactor of claim 7, further comprising:

a first type lightly doped region, disposed in the second type substrate adjacent to the first type second doped region ; and

a second type lightly doped region, disposed in the second type substrate adjacent to the second type second doped region.

14. The differential varactor of claim 13, further comprising:

a spacer, disposed over a sidewall of each of the second gate structures covering the first type lightly doped region and the second type lightly doped region.